AMENDMENTS TO THE SPECIFICATION

On page 7 of the present specification, please replace lines 19-24 with the following paragraph.

This assists in potential contention between the write and read controllers [[21,]] 22, 23 and also assists later in that, when the dispatch unit 5 sends a request to the memory hub for a particular packet, the request first comes to a datagram retrieval unit DRU, such as [[24]]26 in Figure 2, which then issues the request to each channel in turn. There is, therefore, distribution on the read side as well as on the write side. This further enhances load spreading.